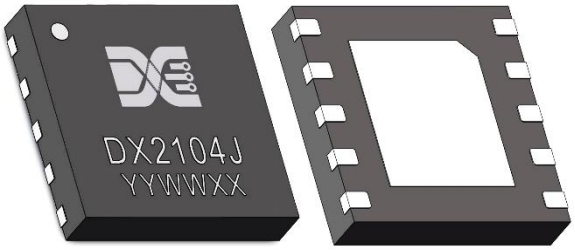
Contents

DX2104 80V 1.5A、5A Half-Bridge GaN Driver

1. Features

- Independent High-Side and Low-Side TTL Logic Inputs
- Separate output realizes adjustable turn on/off strength
- 1.5A/5A peak source/sink current
- 0.5Ω/1.7Ω pull-down/pull-up resistor
- Fast propagation time (Typ. 25ns)
- Excellent propagation delay matching (Typ. 1ns)
- Support positive and negative phase configuration
- Power rail UVLO
- Low power consumption



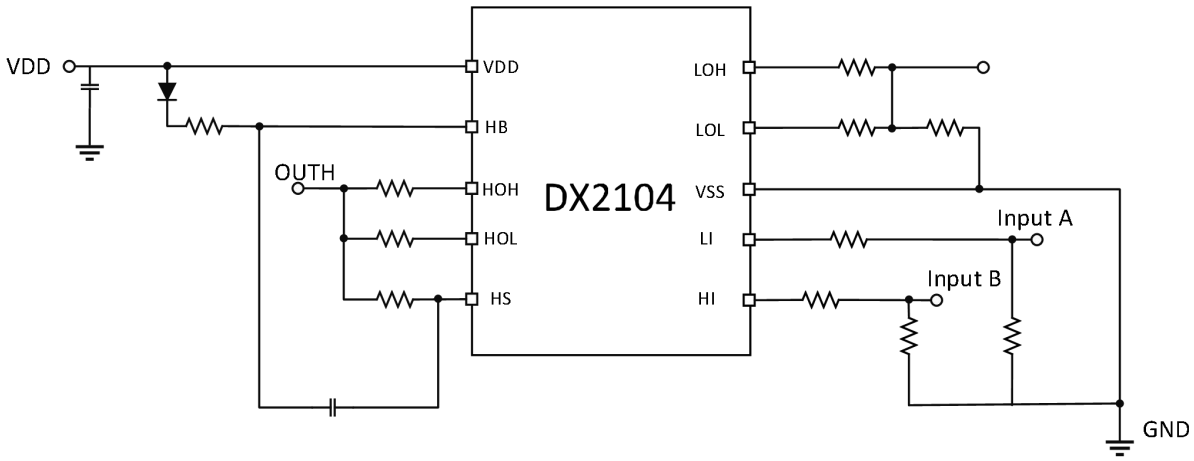
2. Device Information

Part Number	Package	Packing
DX2104J	DFN4x4（mm）	Tape，4000 k/reel

3. Applications

- Mobile Wireless Chargers
- Audio Power Amplifiers
- Audio Power Supplies
- Current-Fed Push-Pull Converters
- Half- and Full-Bridge Converters
- Synchronous Buck Converters

Typical Application Diagram



4. Truth Table

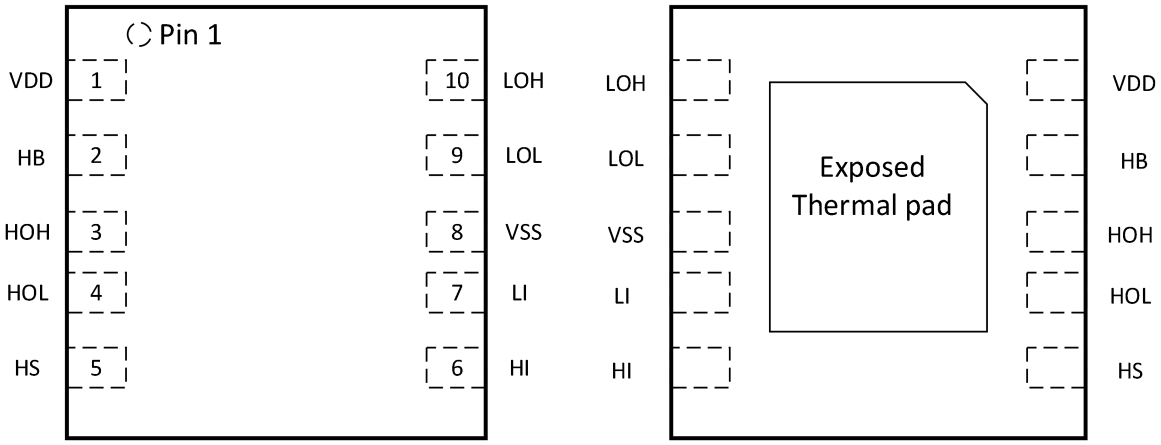
HI	LI	HOH	HOL	LOH	LOL
L	L	OPEN	L	OPEN	L
L	H	OPEN	L	H	OPEN
H	L	H	OPEN	OPEN	L
H	H	H	OPEN	H	OPEN

5. Description

The DX2104 device is designed to simultaneously drive high-side and low-side E-mode GaN HEMT in synchronous buck or half-bridge configurations. The floating high-side driver can drive E-mode GaN HEMT with operating voltage up to 80V. The high-side bias voltage is internally clamped at 5.2V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of E-mode GaN HEMT. The input of the DX2104 is TTL logic compatible, it can withstand input voltage up to 14 V regardless of the VDD voltage. DX2104 has split-gate output, which can flexibly and independently adjust the intensity of turn-on and turn-off. In addition, the strong sink capability of the DX2104 maintains the gate in the low state, which can prevent unintended turn on during switching. It can operate up to several MHz. The DFN4x4

package contains an exposed pad to aid power dissipation.

6. Pin Configuration and Functions



DFN4x4 Top View DFN4x4 Bottom View

Symbol	Describe	Application information
VDD	Positive gate drive supply	VDD 5V: locally decouple to VSS using low ESR/ESL capacitor located as close to the IC as possible.
HB	Bootstrap high-side gate driver supply	Bootstrap capacitor: Connects the positive terminal to HB and the negative terminal to HS; Placed as close to the IC as possible
HOH	High-side gate driver turn-on output	Connect to the gate of high-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turn on speed
HOL	High-side gate driver turnoff output	Connect to the gate of high-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turn off speed
HS	High-side GaN FET source connection	Connect to the bootstrap capacitor negative terminal and the source of the high-side GaN FET
HI	High-side driver control input	The IC inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
LI	Low-side driver control input.	The IC inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
VSS	Ground return	All signals are referenced to this ground.
LOL	Low-side gate driver sink-current output	Connect to the gate of the low-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turnoff speed.

LOH	Low-side gate driver source-current output	Connect to the gate of high-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turnon speed.
EP	Exposed Pad	Recommends that the exposed pad on the bottom of the package be soldered to ground plane on the printed-circuit board to aid thermal dissipation.

7. Key Technical Indicators

7.1 Absolute Maximum Ratings

Over operating free-air temperature range(Unless otherwise noted) (1)

Description	Min	Max	Unit
VDD to VSS	-0.3	5.5	V
HB to HS	-0.3	5.5	V
LI or HI input	-0.3	15	V
LOH, LOL output	-0.3	VDD + 0.3	V
HOH, HOL output	V_{HS} - 0.3	V_{HB} + 0.3	V
HS to VSS	-0.5	94.5	V
HB to VSS	0	V_{HS} + 5.5	V
Operating junction temperature		125	℃
Storage temperature, Tstg	-55	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions.* Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

Symbol	Description	Value	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	V

7.3 Recommended Operating Conditions

Over operating free-air temperature range(Unless otherwise noted)

Description	Min	Max	Unit
VDD	4.5	5	V
LI or HI input	0	14	V
HS	-5	80	V
HB	V_{HS}+4	V_{HS}+5	V
HS slew rate		50	V/ns
Operating junction temperature	-40	125	℃

7.4 Thermal Characteristics

Symbol	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.5	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.8	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	℃/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	℃/W
ψ_{JB}	Junction-to-board characterization parameter	14.9	℃/W
$R_{\theta JC(bottom)}$	Junction-to-board thermal resistance	4.1	℃/W

7.5 Electrical Characteristics

Specifications are T_j=25°C. Unless otherwise specified: VDD=VHB=5 V, VSS=VHS=0 V.

No load on LOL and HOL or HOH and HOL(1).

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
Supply Currents						
I_{DD}	VDD quiescent current	LI = HI = 0 V		0.3	0.4	mA
I_{DDO}	VDD operating current	f=500kHz		2.0	3.0	mA
I_{HB}	Total HB quiescent current	Total HB quiescent current		0.14	0.16	mA
I_{HBO}	Total HB operating current	f=500kHz		1.5	2.5	mA
I_{HBS}	HB to VSS quiescent current	HS = HB = 100 V		0.1	8	μA
I_{HBSO}	HB to VSS operating current	f=500kHz		0.4	1	mA
Input Pins						
V_{IR}	Input voltage threshold	Rising edge	1.90	2.08	2.20	V
V_{IF}	Input voltage threshold	Falling edge		1.68	1.78	V
V_{IHYS}	Input voltage hysteresis	V_{IR}- V_{IF}		400		mV
R_I	Input pulldown resistance	T_j=25°C		200		kΩ
Undervoltage protection						
V_{DDR}	VDD rising threshold	T_j=25°C	2.4	2.6	3	V
V_{DDH}	VDD threshold hysteresis	T_j=25°C		0.2		V
V_{HBR}	HB rising threshold	T_j=25°C		2.55		V
V_{HBH}	HB threshold hysteresis	T_j=25°C		0.2		V

Bootstrap Diode						
V_{DL}	Low-current forward voltage	I_{VDD-HB} = 500 μA		0.42		V
V_{DH}	High-current forward voltage	I_{VDD-HB} = 2 mA		0.52		V
	HB-HS clamp	Regulation voltage		5.2		V

（1）Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
Low and High side Gate Driver						
V_{OL}	Low-level output voltage	I_{HOL} = I_{LOL} = 100 mA		0.043		V
V_{OH}	High-level output voltage V_{OH} = VDD-LOH Or V_{OH}=HB-HOH	I_{HOL} = I_{LOL} = 100 mA		0.166		V
I_{OHL}	Peak source current	HOH, LOH = 0 V		1.5		A
I_{OLL}	Peak sink current	HOL, LOL = 5 V		5		A
I_{OHL}	High-level output leakage current	HOH, LOH = 0 V			1.5	uA
I_{OLLK}	Low-level output leakage current	HOL, LOL = 5 V			1.5	uA

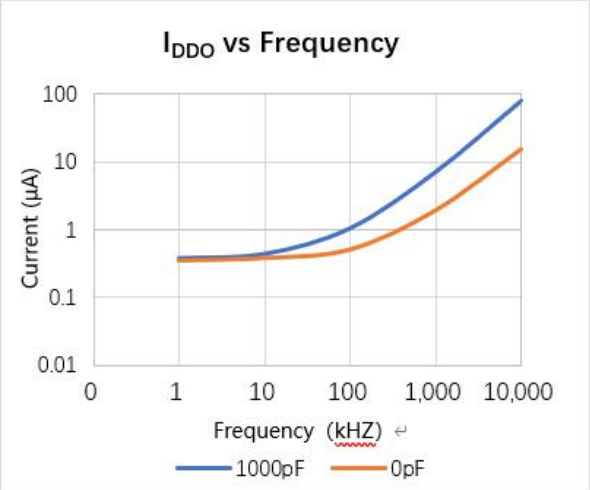
7.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

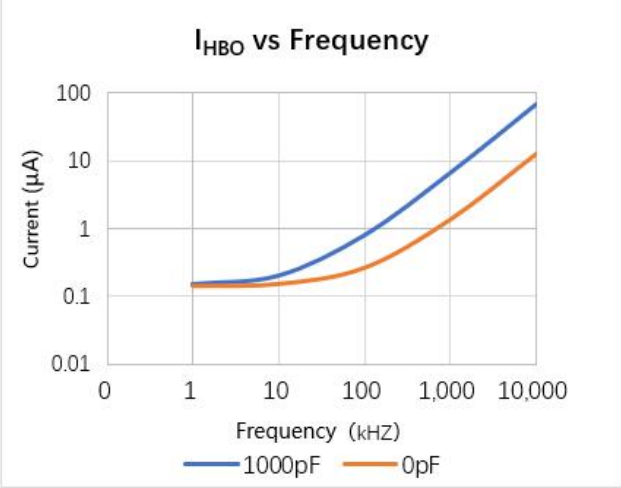
Symbol	Description	Conditions	Min.	Typ.	Max.	Units
Low and High side Gate Driver						
t_{LPHL}	LO turnoff propagation delay	LI falling to LOL failing		34		ns
t_{LPLH}	LO turnon propagation delay	LI rising to LOL failing		20		ns

t_{HPHL}	HO turnoff propagation delay	HI falling to HOL failing		35		ns
t_{HPLH}	HO turnon propagation delay	HI rising to HOL failing		20		ns
t_{MON}	Delay matching LO on & HO off	T_J=25℃		0.5		ns
T_{MOFF}	Delay matching LO off & HO on	T_J=25℃		0.6		ns
t_{HRC}	HO rise time(0.5V-4.5V)	C_L=1000pF		7.1		ns
t_{LRC}	LO rise time(0.5V-4.5V)	C_L=1000pF		8.2		ns
T_{HFC}	HO rise time(0.5V-4.5V)	C_L=1000pF		5.6		ns
T_{LFC}	LO rise time(0.5V-4.5V)	C_L=1000pF		6.1		ns
t_{PW}	Minimum input pulse width that changes the output	C_L=1000pF		16		ns

8. Characteristic curves



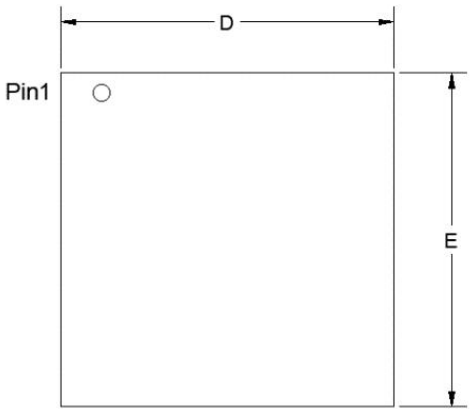
Picture 1. I_{DDO} vs Frequency



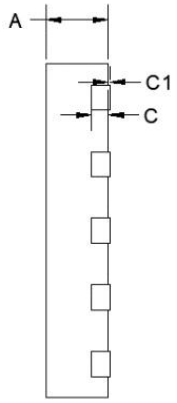
Picture 2. I_{HBO} vs Frequency

9. Package

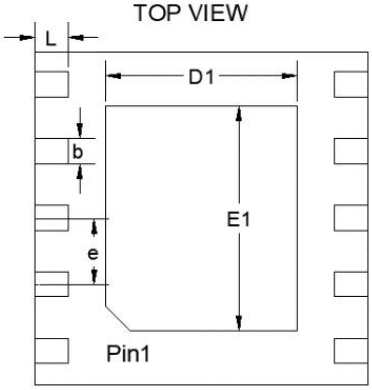
Dimensions(mm)			
Symbol	Min.	Typ.	Max.
A	0.70	0.75	0.80
B	0.25	0.30	0.35
D	3.90	4.00	4.10
D1	2.20	2.30	2.40
E	3.90	4.00	4.10
E1	2.70	2.70	2.80
e	REF 0.8		
L	0.30	0.40	0.50



TOP VIEW



SIDE VIEW



BOTTOM VIEW

10. Product packaging

ITEM	W	Ao	Bo	Ko	E	F	D1	D0	P0	P1	P2	T
MIN	11.70	4.15	4.15	0.95	1.65	5.40	—	—	3.90	7.90	1.90	0.18
NOM	12.00	4.25	4.25	1.05	1.75	5.50	1.50	1.50	4.00	8.00	2.00	0.23
MAX	12.30	4.35	4.35	1.15	1.85	5.60	1.60	1.60	4.10	8.10	2.10	0.28