
DX65T200 E-mode 650V,10A,200mΩ GaN HEMT

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1. FEATURES

- 650 V enhancement mode power switch
- $R_{DS(on)} = 200m\Omega$
- $I_{DS(max)} = 10A$
- Easy gate drive requirements (0 V to 6 V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Zero reverse recovery loss



2. Applications

- Fast Battery Charging
- LED lighting drivers
- Power Factor Correction
- LLC Converters
- Wireless Power Transfer

Device Information

Part Number	Package	Quantity
DX65T200	TO-220F	50

3. Description

DX65B200 is an enhancement mode GaN-on-silicon transistor. GaN is a wide band gap semiconductor with high power density. The gallium nitride transistor is characterized by no body diode, so the reverse recovery charge is zero.

4. Absolute Maximum Ratings($T_c=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit	Condition
Drain-Source voltage	V_{DS}	650	V	
Gate-source voltage	V_{GS}	-10 to 6	V	
Continuous drain current*	I_D	10	A	$T_c=25^{\circ}\text{C}$
		4.5	A	$T_c=125^{\circ}\text{C}$
Operation and storage temperature	T_j	-55 to 150	$^{\circ}\text{C}$	
	T_{stg}	-55 to 150	$^{\circ}\text{C}$	

5. Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise specified)

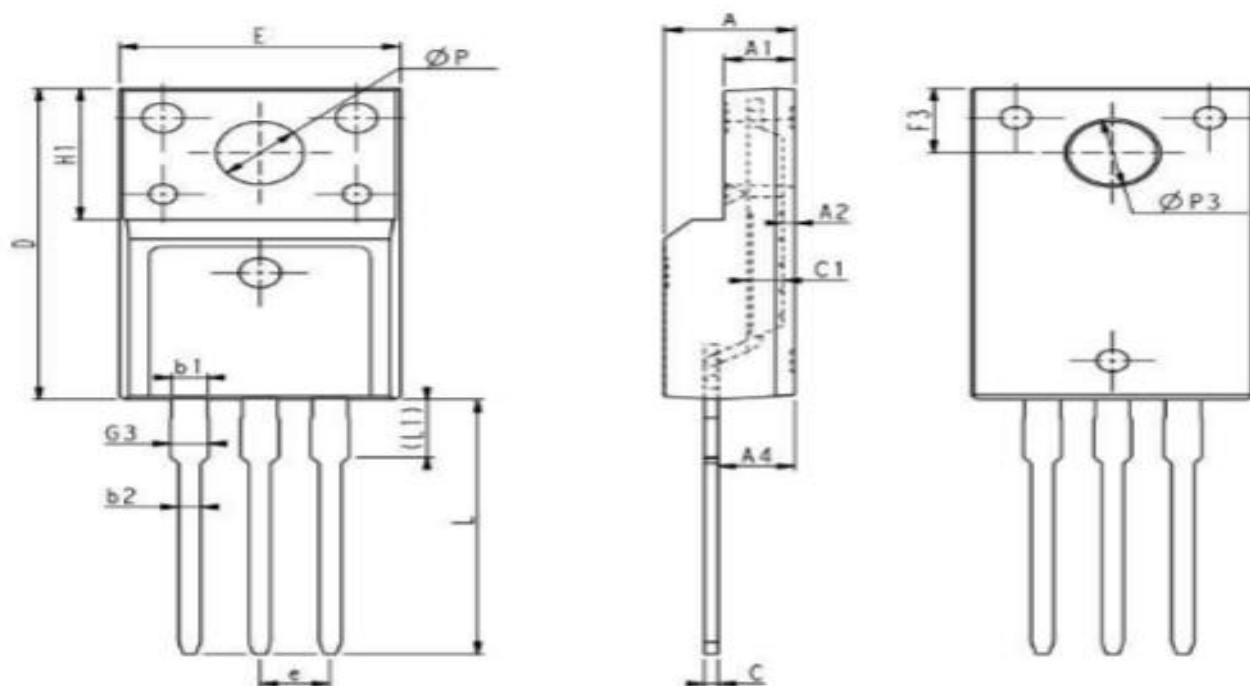
5.1 Typical Performance – Static

Parameter	Symbol	Values			Unit	Test condition
		Min.	Type.	Max.		
Drain source breakdown voltage	BV_{DS}	650	/	/	V	$V_{GS}=0V$, $I_D=20\mu A$
Total drain leakage current	I_{DSS}	/	1	10	μA	$V_{DS}=650V$, $V_{GS}=0V$, $T_j=25^{\circ}\text{C}$
		/	8	110	μA	$V_{DS}=650V$, $V_{GS}=0V$, $T_j=150^{\circ}\text{C}$
Gate-to-source current	I_{GS}	/	10	/	μA	$V_{DS}=0V$, $V_{GS}=6V$, $T_j=25^{\circ}\text{C}$
Static drain-source on-resistance	$R_{DS(ON)}$	/	150	200	$m\Omega$	$V_{GS}=6V$, $I_D=3A$, $T_j=25^{\circ}\text{C}$
		/	300	/	$m\Omega$	$V_{GS}=6V$, $I_D=3A$, $T_j=150^{\circ}\text{C}$
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.0	V	$V_{DS}=V_{GS}$, $I_D=3.5mA$,

5.2 Typical Performance – Dynamic

Parameter	Symbol	Values			Unit	Test condition
		Min	Type	Max		
Input capacitance	C_{ISS}	/	72	/	pF	$V_{DS}=400V$, $V_{GS}=0V$, $f=1MHz$
Output capacitance	C_{OSS}	/	20	/	pF	
Reverse transfer capacitance	C_{RSS}	/	0.2	/	pF	
Output capacitance, energy related	$C_{OSS(er)}$	/	31	/	pF	$V_{DS}=0V$ to $400V, V_{GS}=0V$
Output capacitance time related	$C_{OSS(tr)}$	/	44	/	pF	
Total gate charge	Q_G	/	2.4	/	nC	$V_{DS}=400V$, $V_{GS}=0V$ to $6V$
Gate-drain charge	Q_{GD}	/	0.25	/	nC	
Gate-source charge	Q_{GS}	/	1.1	/	nC	
Gate Resistance	R_G	/	1.95	/	Ω	$f = f_{res}$, Open drain

6. Package



COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
E	9.96	10.16	10.36
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A2	0.30	0.45	0.60
A4	2.56	2.76	2.96
c	0.40	0.50	0.65
c1	1.20	1.30	1.35
D	15.57	15.87	16.17
H1	6.70REF		
e	2.54BSC		
L	12.68	12.98	13.28
L1	2.93	3.03	3.13
ΦP	3.03	3.18	3.38
ΦP3	3.15	3.45	3.65
F3	3.15	3.30	3.45
G3	1.25	1.35	1.55
b1	1.18	1.28	1.43
b2	0.70	0.80	0.95