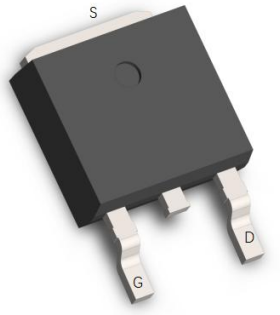
DX65B400 E-mode 650V,7A,400mΩ GaN HEMT

Contents

1. Features

- 650 V enhancement mode power switch
- $R_{DS(on)}$ =400mΩ
- $I_{DS(max)}$ = 7A
- Easy gate drive requirements (0 V to 6 V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Zero reverse recovery loss



2. Applications

- Fast Battery Charging
- LED lighting drivers
- Power Factor Correction
- LLC Converters
- Wireless Power Transfer

Device Information

Part Number	Package	Packing
DX65B400	TO252	Tape 2.5k/reel

3. Description

DX65B400 is an enhancement mode GaN-on-silicon transistor. GaN is a wide band gap semiconductor with high power density. The gallium nitride transistor is characterized by no body diode, so the reverse recovery charge is zero.

4. Absolute Maximum Ratings(Tc=25℃ unless otherwise specified)

Parameter	Symbol	Value	Unit	Condition
Drain-Source voltage	V_{DS}	650	V	
Gate-source voltage	V_{GS}	-10 to 6	V	
Continuous drain current*	I_D	7	A	Tc=25℃
		4	A	Tc=125℃
Operation and storage temperature	Tj	-55 to 150	℃	
	Tstg	-55 to 150	℃	

5. Electrical Characteristics (Tc=25℃ unless otherwise specified)

5.1 Typical Performance – Static

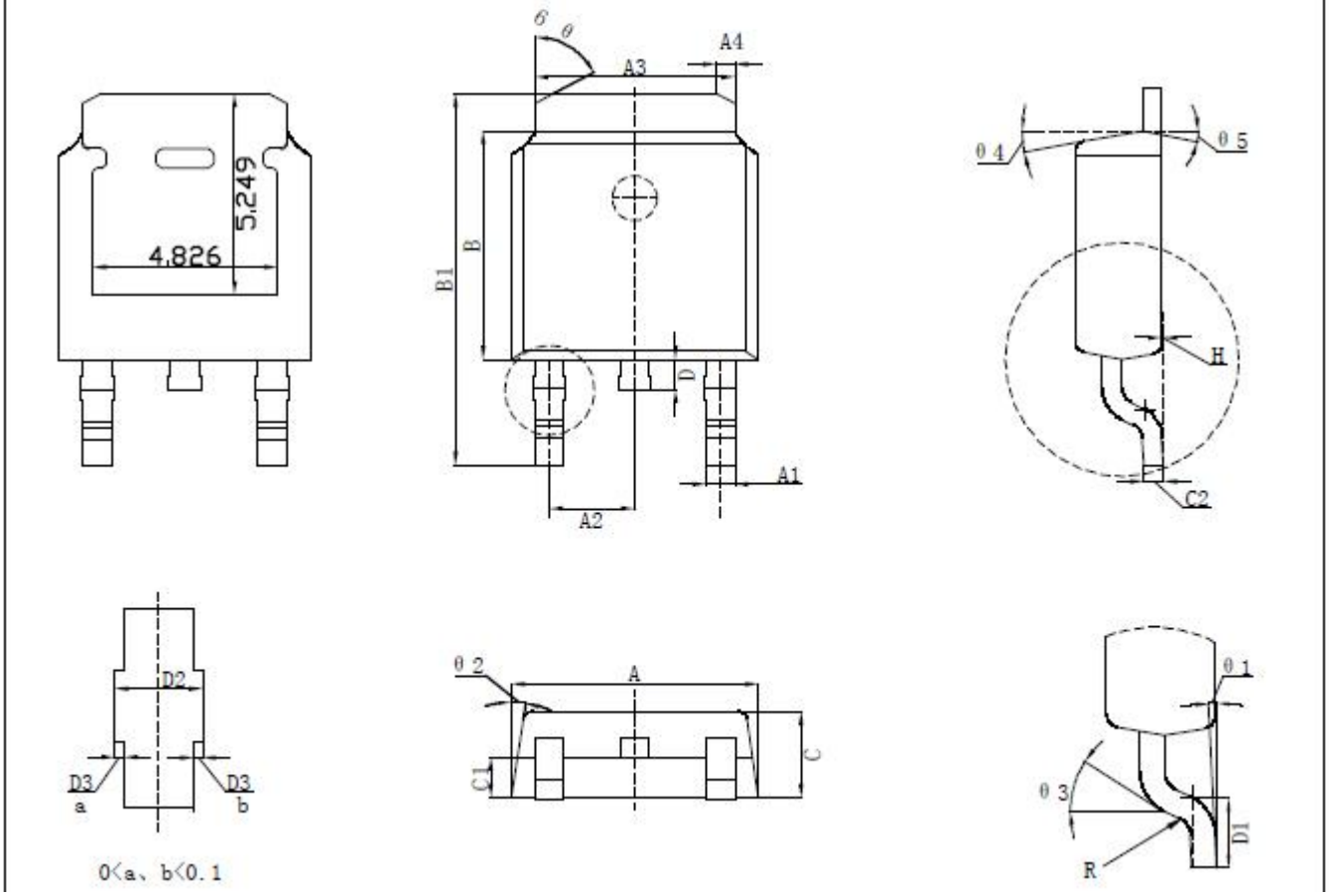
Parameter	Symbol	Values			Unit	Test condition
		Min.	Type.	Max.		
Drain source breakdown voltage	BV_{DS}	650	/	/	V	VGS=0V, ID=20μA
Total drain leakage current	I_{DSS}	/	0.3	10	μA	VDS=650V, VGS=0V, Tj=25℃
		/	5	75	μA	VDS=650V, VGS=0V, Tj=150℃
Gate-to-source current	I_{GS}	/	2	/	μA	VDS=0V, VGS=6V, Tj=25℃
Static drain-source on-resistance	$R_{DS(ON)}$	/	350	400	mΩ	VGS=6V, ID=3A, Tj=25℃
		/	650	/	mΩ	VGS=6V, ID=3A, Tj=150℃
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.0	V	VDS=VGS, ID=3.5mA ,

5.2 Typical Performance – Dynamic

Parameter	Symbol	Values			Unit	Test condition
		Min	Type	Max		
Input capacitance	C_{ISS}	/	32	/	pF	V_{DS}=400V, V_{GS}=0V, f=1MHz
Output capacitance	C_{OSS}	/	9	/	pF	
Reverse transfer capacitance	C_{RSS}	/	0.3	/	pF	
Output capacitance, energy related	$C_{OSS(er)}$	/	15	/	pF	V_{DS}=0V to 400V,V_{GS}=0V
Output capacitance time related	$C_{OSS(tr)}$	/	21	/	pF	
Total gate charge	Q_G	/	1.3	/	nC	V_{DS}=400V, V_{GS}=0V to 6V
Gate-drain charge	Q_{GD}	/	0.33	/	nC	
Gate-source charge	Q_{GS}	/	0.6	/	nC	
Gate Resistance	R_G	/	2.88	/	Ω	*f* = *f*res, Open drain

6. Package

尺寸 / 标注	最小(mm)	最大(mm)	尺寸 / 标注	最小(mm)	最大(mm)
A	6.50	6.70	D1	1.40	1.60
A1	0.71	0.81	D2	0.81	0.91
A2	2.236	2.336	D3	0.05TYP	
A3	5.284	5.384	H	0.00	0.10
A4	0.75	0.85	R	0.40TYP	
B	6.00	6.20	θ1	0°	8°
B1	9.80	10.10	θ2	8.5° TYP4	
C	2.20	2.40	θ3	25° TYP	
C1	0.967	1.087	θ4	10° TYP2	
C2	0.498	0.518	θ5	10° TYP	
D	0.70	0.90	θ6	70° TYP	



7. Packing

ITEM	W	Ao	Bo	B_1	B_2	Ko	K_1	E	F	D_1	D_0	P_0	P_1	P_2	t
MIN	16.30	6.80	10.40	2.15	7.50	2.50	0.65	1.65	7.45	—	—	3.90	7.90	1.90	0.20
NOM	16.00	6.90	10.50	2.20	7.55	2.60	0.70	1.75	7.50	1.50	1.50	4.00	8.00	2.00	0.25
MAX	15.90	7.00	10.60	2.25	7.60	2.70	0.75	1.85	7.55	1.60	1.60	4.10	8.10	2.10	0.30