

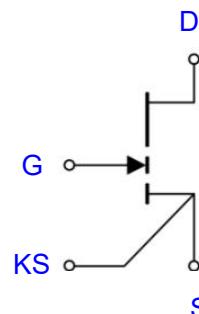
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DX65x200 E-mode 650V,10A,200mΩ GaN HEMT

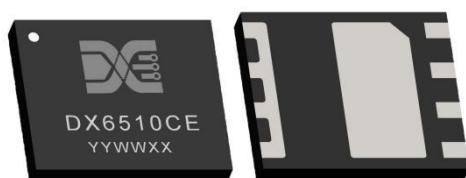
1. Features

- 650 V enhancement mode power switch
- $R_{DS(on)} = 200m\Omega$
- $I_{DS(max)} = 10A$
- Easy gate drive requirements (0 V to 6 V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Zero reverse recovery loss

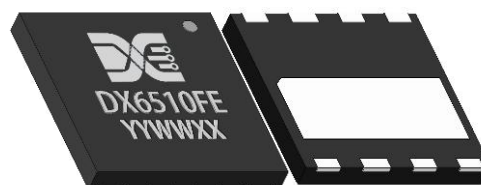


2. Device Information

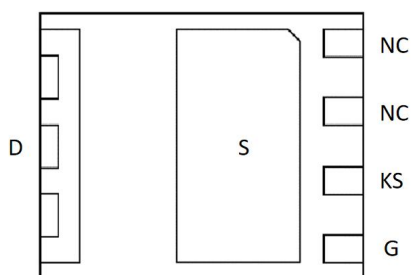
Part Number	Marking Code	Package	Packing
DX65C200	DX6510CE	DFN5x6	Tape 4000pcs/reel
DX65F200	DX6510FE	DFN8x8	260pcs/tray



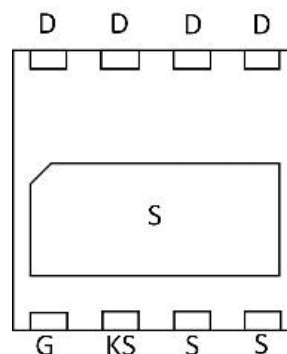
DX65C200 DFN5x6



DX65F200 DFN8x8



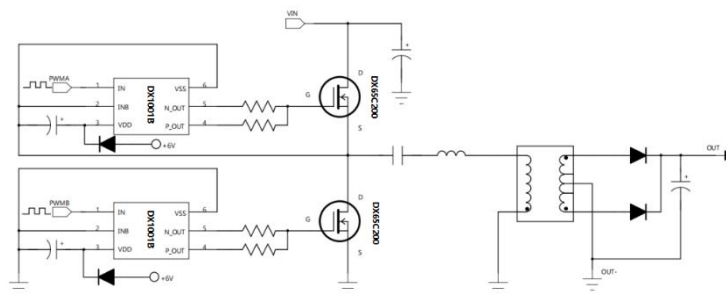
DX65C200 Bottom View



DX65F200 Bottom View

3. Applications

- Fast Battery Charging
- LED lighting drivers
- Power Factor Correction
- LLC Converters
- Wireless Power Transfer



Typical application circuit of LLC

4. Description

DX65x200 is an enhancement mode GaN-on-silicon transistor. GaN is a wide band gap semiconductor with high power density. The gallium nitride transistor is characterized by no body diode, so the reverse recovery charge is zero.

5. Absolute Maximum Ratings (Tc=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit	Condition
Drain-Source voltage	V_{DS}	650	V	
Gate-source voltage	V_{GS}	-10 to 6	V	
Continuous drain current*	I_D	10	A	Tc=25°C
		4.5	A	Tc=125°C
Operation and storage temperature	T_j	-55 to 150	°C	
	T_{stg}	-55 to 150	°C	

* An Estimated Value

6. Electrical Characteristics (Tc=25°C unless otherwise specified)

6.1 Typical Performance – Static

Parameter	Symbol	Values			Unit	Test condition
		Min.	Type.	Max.		
Drain source breakdown voltage	BV_{DS}	650	/	/	V	$V_{GS}=0V, I_D=200\mu A$
Total drain leakage current	I_{DSS}	/	1	10	μA	$V_{DS}=650V, V_{GS}=0V, T_j=25^\circ C$
		/	8	110	μA	$V_{DS}=650V, V_{GS}=0V, T_j=150^\circ C$
Gate-to-source current	I_{GSS}	/	10	/	μA	$V_{DS}=0V, V_{GS}=6V, T_j=25^\circ C$
Static drain-source on-resistance	$R_{DS(ON)}$	/	150	200	m Ω	$V_{GS}=6V, I_D=3A, T_j=25^\circ C$
		/	300	/	m Ω	$V_{GS}=6V, I_D=3A, T_j=150^\circ C$
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.0	V	$V_{DS}=V_{GS}, I_D=3.5mA$

Thermal characteristics (DFN5x6)

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction-ambient	R_{thJA}	60.8	$^\circ C/W$	
Thermal resistance, junction-case	R_{thJC}	1.72	$^\circ C/W$	
Maximum reflow soldering temperature	T_{sold}	260	$^\circ C$	MSL3

Thermal characteristics (DFN8x8)

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction-ambient	R_{thJA}	58.5	$^\circ C/W$	
Thermal resistance, junction-case	R_{thJC}	1.72	$^\circ C/W$	
Maximum reflow soldering temperature	T_{sold}	260	$^\circ C$	MSL3

6.2 Typical Performance – Dynamic

Parameter	Symbol	Values			Unit	Test condition
		Min	Type	Max		
Input capacitance	C_{ISS}	/	72	/	pF	$V_{DS}=400V$, $V_{GS}=0V$, $f=1MHz$
Output capacitance	C_{OSS}	/	20	/	pF	
Reverse transfer capacitance	C_{RSS}	/	0.2	/	pF	
Output capacitance, energy related	$C_{OSS(er)}$	/	31	/	pF	$V_{DS}=0V$ to $400V, V_{GS}=0V$
Output capacitance time related	$C_{OSS(tr)}$	/	44	/	pF	
Total gate charge	Q_G	/	2.4	/	nC	$V_{DS}=400V$, $V_{GS}=0V$ to $6V$
Gate-drain charge	Q_{GD}	/	0.25	/	nC	
Gate-source charge	Q_{GS}	/	1.1	/	nC	
Gate Resistance	R_G	/	1.95	/	Ω	$f = f_{res}$, Open drain
Turn-on delay time	$t_{d(on)}$	/	2	/	nS	$V_{DS}=400V$; $I_D=6A$; $L=318\mu H$; $V_{GS}=6V$ $R_{on}=10\Omega$; $R_{off}=2\Omega$;
Turn-off delay time	$t_{d(off)}$	/	4	/	nS	
Rise time	t_r	/	5	/	nS	
Fall time	t_f	/	6	/	nS	

6.3 Characteristic Curve

Figure 1 Typ. output characteristics

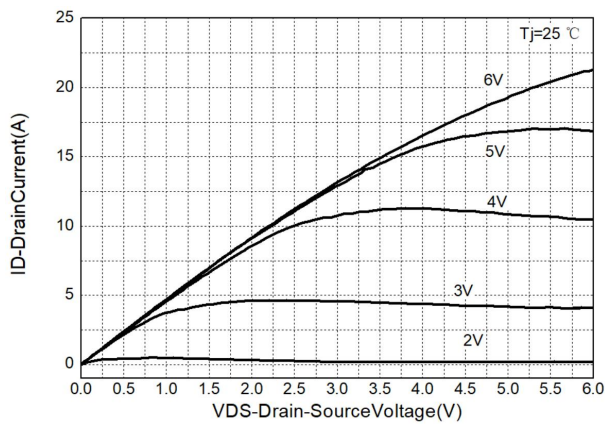


Figure 2 Typ. Drain-source on-state resistance

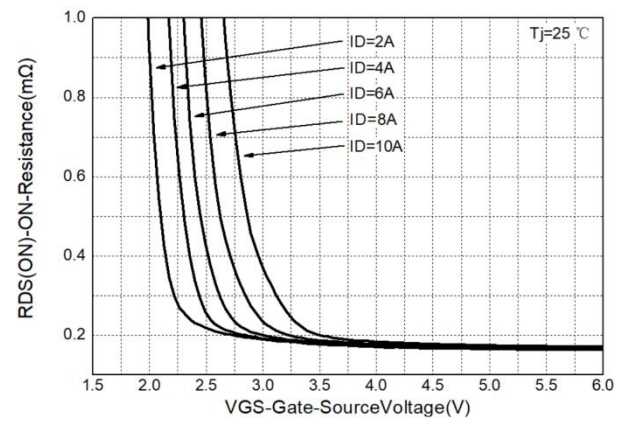


Figure 3 Typ. channel reverse characteristics

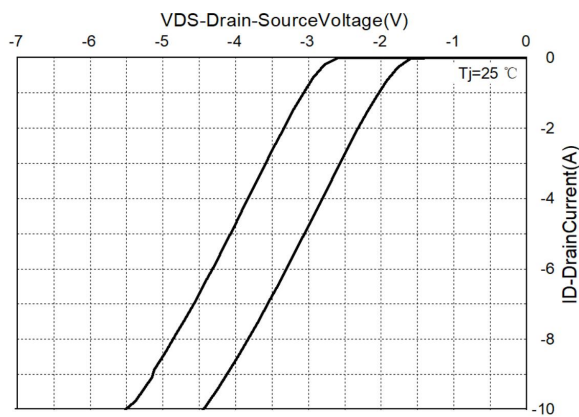


Figure 4 Typ. transfer characteristics

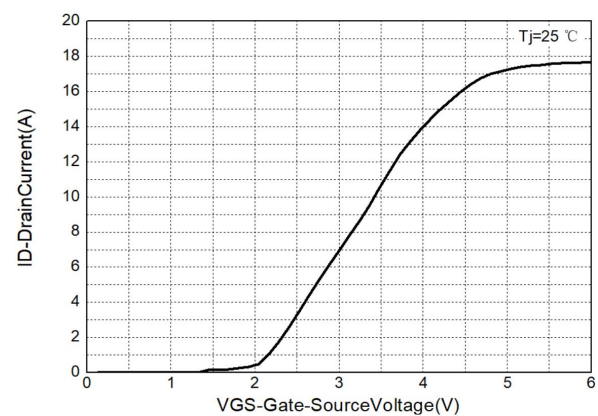


Figure 5 Typ. Gate threshold voltage

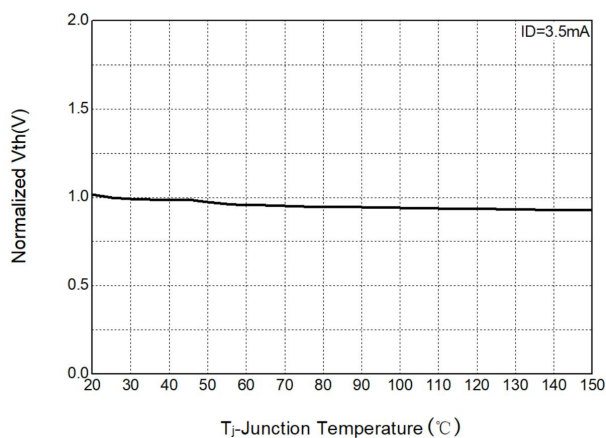


Figure 6 Typ. Drain-source on-state resistance

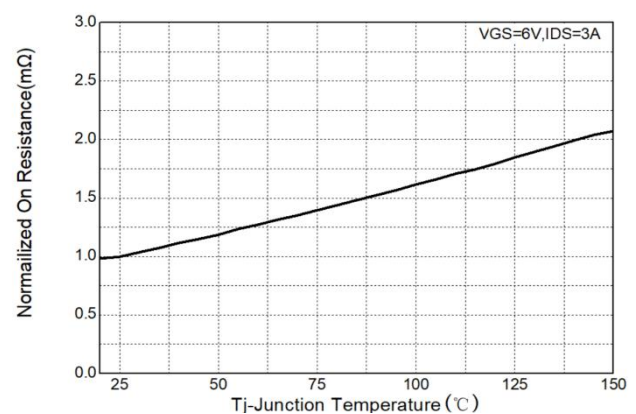


Figure 7 Typ.Drain-source leakage characteristics

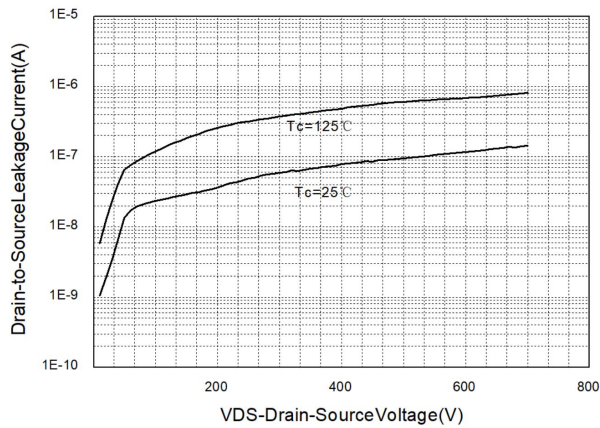


Figure 8 Typ. gate charge

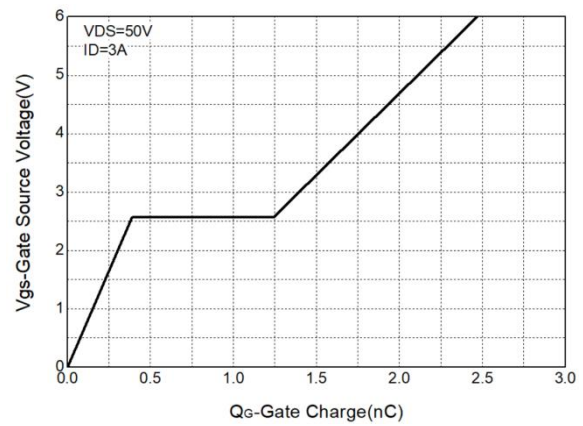


Figure 9.1 Safe operating area (DFN5x6)

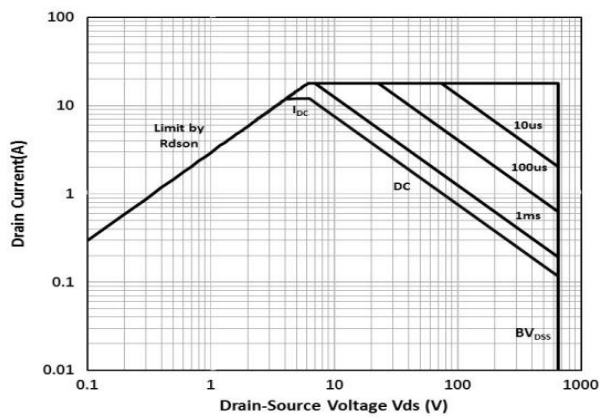


Figure 10.1 Max.transient thermal impedance (DFN5x6)

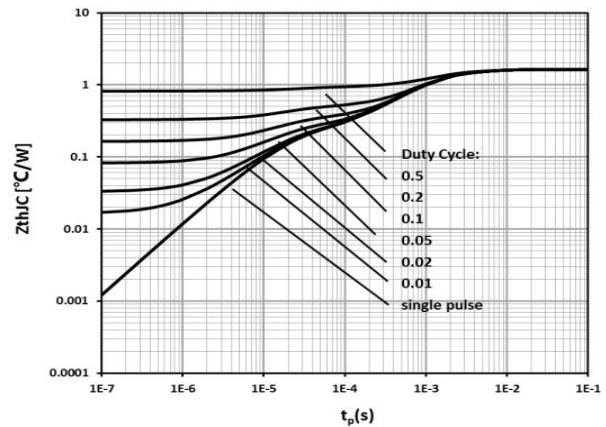


Figure 9.2 Safe operating area (DFN8x8)

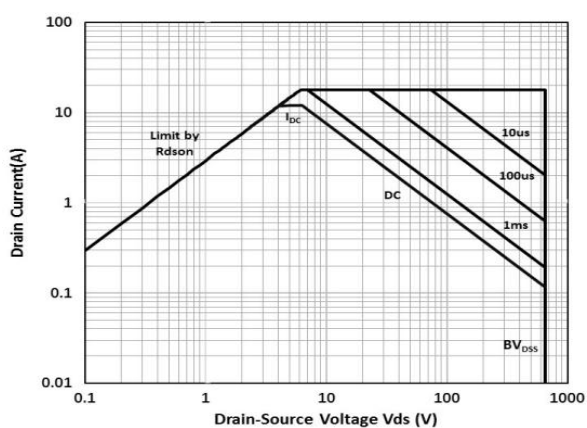


Figure 10.2 Max.transient thermal impedance (DFN8x8)

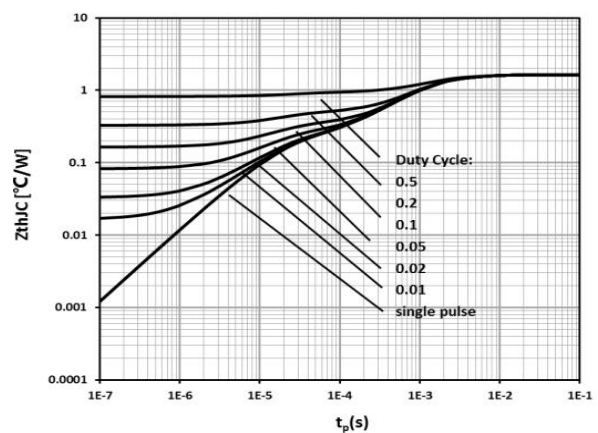


Figure 11 Power dissipation

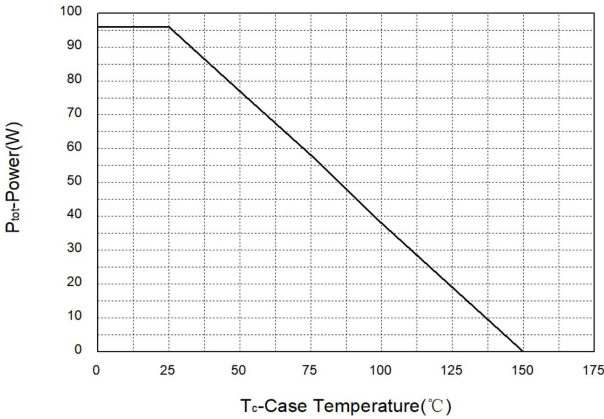
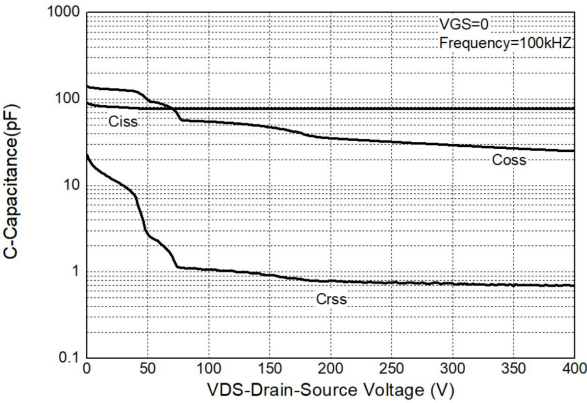


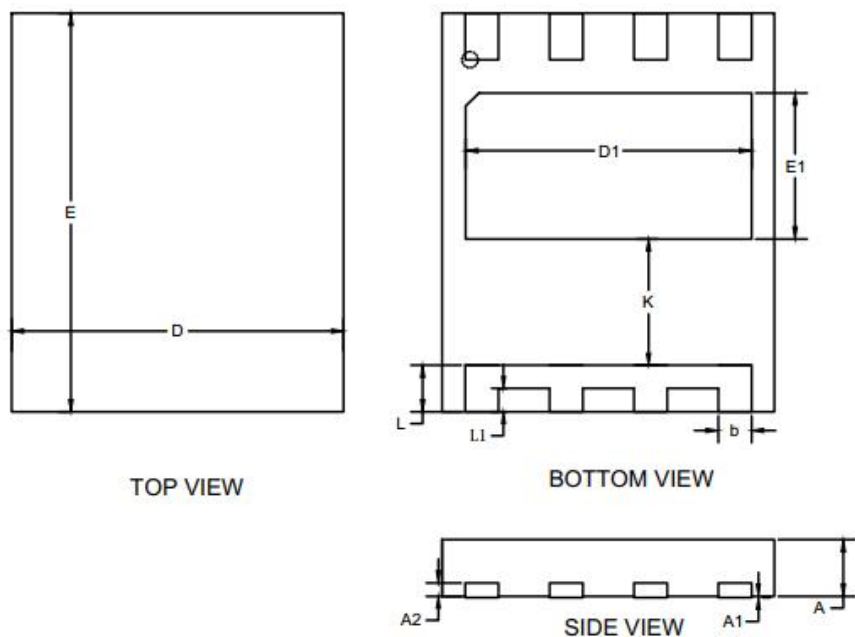
Figure 10 Capacitances



7. Package Outline Dimensions

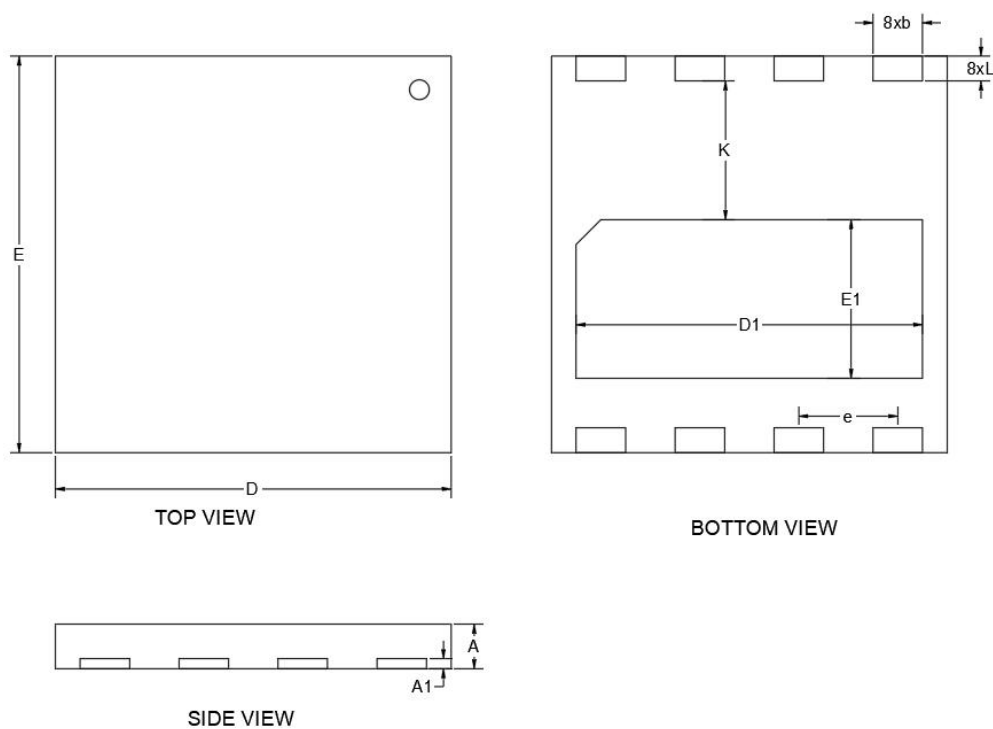
7.1 DFN5x6

Dimensions(mm)			
Symbol	Min.	Nom.	Max.
A	0.8	0.85	0.9
A1	-	0.02	0.05
A2	0.2(REF)		
b	0.45	0.50	0.55
D	4.90	5.00	5.10
D1	4.20	4.30	4.40
E	5.90	6.00	6.10
E1	2.10	2.20	2.30
e	1.27		
k	1.9	-	-
L	0.65	0.7	0.75



7.2 DFN8x8

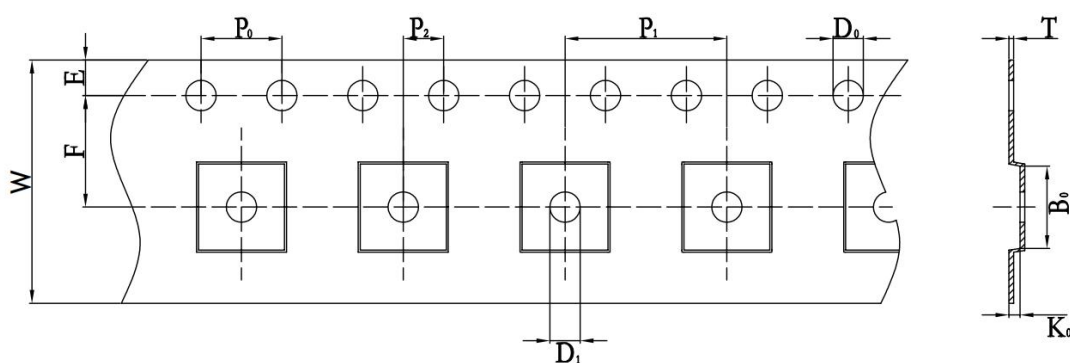
Dimensions(mm)			
Symbol	Min.	Nom.	Max.
A	0.80	0.90	1.00
A1	REF 0.203		
b	0.95	1.00	1.05
D	7.90	8.00	8.10
D1	6.90	7.00	7.10
E	7.90	8.00	8.10
E1	3.10	3.20	3.30
e	REF 2.00		
k	REF 2.80		
L	0.45	0.50	0.55



8. Product packaging

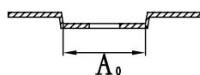
8.1 DFN5x6

ITEM	W	Ao	Bo	Ko	E	F	D1	D0	P0	P1	P2	T
MIN	11.70	4.15	4.15	0.95	1.65	5.40	—	—	3.90	7.90	1.90	0.18
NOM	12.00	4.25	4.25	1.05	1.75	5.50	1.50	1.50	4.00	8.00	2.00	0.23
MAX	12.30	4.35	4.35	1.15	1.85	5.60	1.60	1.60	4.10	8.10	2.10	0.28

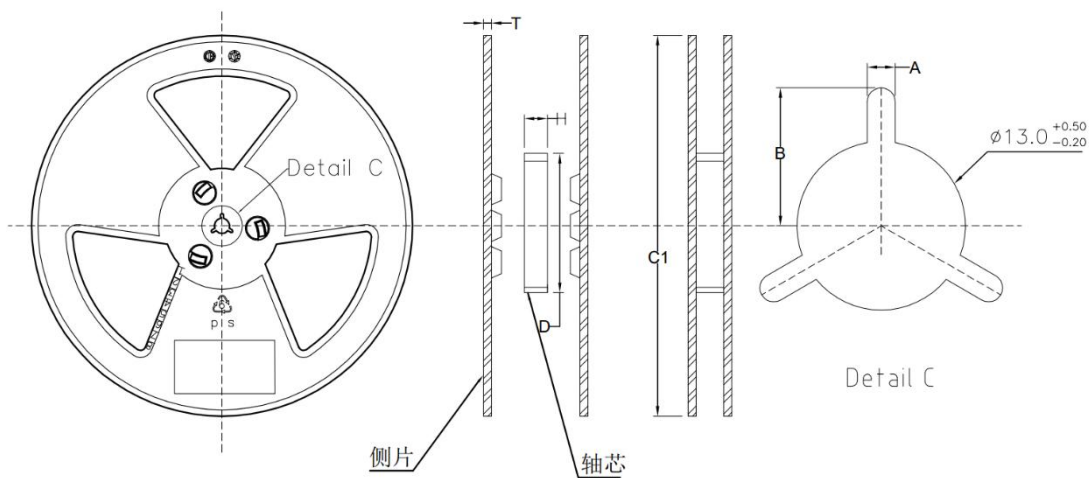


USER FEED DIRECTION

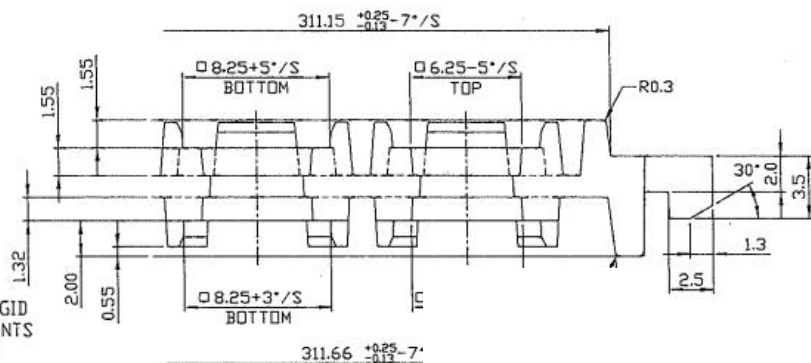
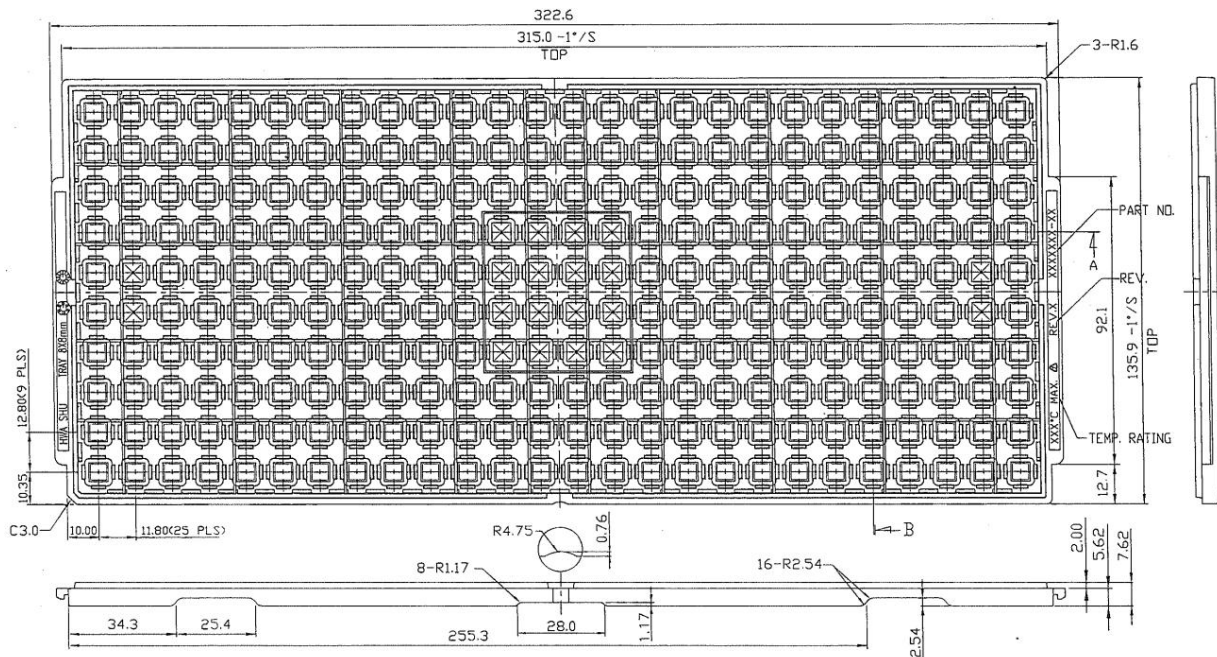
进料方向



产品符合ROHS 环境管理物质标准



8.2 DFN8x8



NOTES :

1. (S.R. OHM/SQ.) MEANS SURFACE ELECTRIC RESISTIVITY OF THE TRAY.
2. THE MOLDED TRAY'S MATERIAL SHALL BE RIGID ENOUGH TO AVOID DAMAGE TO THE COMPONENTS DURING HANDLING, LOADING, BACKING, TESTING, SHIPPING AND PLACING.
3. TRAYS ARE STACKABLE WITHOUT INTERFERENCE AND WILL NOT STICK TOGETHER DURING UNSTACKING OPERATION.
4. WARPAGE IS WITHIN 0.76 mm.
5. THE CELLS MARKED WITH CROSS SYMBOL ARE FOR VACUUM PICKUP AREA AND WITHOUT THRU HOLES.
6. TOTAL USABLE CELLS 10X26=260.
7. ALL DIMENSIONS ARE IN MILLIMETERS.

SECTION A (4/1)

